Amendments of the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the above-identified patent application:

Listing of Claims

1-29. (canceled)

30. (new) A method of aligning a boundary between bytes of a deserialized serial data signal that has been input into a programmable logic device, said programmable logic device having a serial data interface, and having a programmable logic core, said method comprising:

receiving a serial data signal at said serial data interface;

deserializing said serial data signal, including inserting an initial candidate byte boundary between selected bits of said deserialized data signal;

transmitting said deserialized data signal with said initial candidate byte boundary to said programmable logic core;

processing said deserialized signal with said initial candidate byte boundary in said programmable logic core to validate said initial candidate byte boundary; and

sending a byte alignment error signal from said programmable logic core to said serial data interface when said candidate boundary is determined to be invalid.

31. (new) The method of claim 30 further comprising:

assigning based on said error signal an alternate candidate byte boundary between different selected bits of said deserialized data signal on said serial data interface;

retransmitting said deserialized data signal with said alternate candidate byte boundary from said serial data interface to said programmable logic core; and

reprocessing said retransmitted deserialized data signal with said alternate candidate byte boundary in said programmable logic core to validate said alternate candidate byte boundary.

32. (new) The method of claim 31 wherein:

said error signal indicates a number of bits of discrepancy in said byte boundary; and

said assigning an alternate candidate byte boundary comprises moving said byte boundary by said number of bits of discrepancy.

33. (new) The method of claim 31 wherein:

said assigning an alternate candidate byte boundary comprises moving said byte boundary by one bit; and

said sending, said assigning, said retransmitting and said reprocessing occur iteratively until said reprocessing determines that said alternate candidate byte boundary is correct.

34. (new) A method of aligning a boundary between bytes of a deserialized serial data signal that has been input into a programmable logic device, said programmable logic device having a serial data interface, and having a programmable logic core, said method comprising:

receiving a serial data signal at said serial data interface;

deserializing said serial data signal, including inserting an initial candidate byte boundary between selected bits of said deserialized data signal;

transmitting said deserialized data signal with said initial candidate byte boundary from said serial data interface to said programmable logic core; and

receiving a byte alignment error signal from said programmable logic core at said serial data interface when said candidate boundary is determined in said programmable logic core to be invalid.

35. (new) The method of claim 34 further comprising:

assigning based on said error signal an alternate candidate byte boundary between different selected bits of said deserialized data signal at said serial data interface;

retransmitting said deserialized data signal with said alternate candidate byte boundary from said serial data interface to said programmable logic core; and

again receiving a byte alignment error signal from said programmable logic core at said serial data interface when said candidate boundary is determined in said programmable logic core to be invalid.

36. (new) The method of claim 35 wherein:

said error signal indicates a number of bits of discrepancy in said byte boundary; and

said assigning an alternate candidate byte boundary comprises moving said byte boundary by said number of bits of discrepancy.

37. (new) The method of claim 35 wherein:

said assigning an alternate candidate byte boundary comprises moving said byte boundary by one bit; and

said receiving, said assigning and said retransmitting occur iteratively until said alternate candidate byte boundary is determined in said programmable logic core to be correct.

38. (new) A programmable logic device comprising:

a programmable logic core; and

a serial data interface adapted to receive and deserialize a serial data signal, said serial data interface comprising bit-slipping circuitry adapted to a insert a byte boundary between bits of said deserialized data signal, said bit-slipping circuitry being responsive to a bit-slipping control signal from said programmable logic core.

39. (new) The programmable logic device of claim 38 wherein said bit-slipping circuitry comprises bit-handling circuitry and control circuitry that controls said bit-handling circuitry responsive to said bit-slipping control signal.

40. (new) The programmable logic device of claim 39 wherein:

each byte includes a first number of bits; and

said bit-handling circuitry comprises:

at least one shift register for receiving said serial data, and having capacity to hold a second number of bits greater than said first number of bits, and further having a number of parallel outputs equal to said second number of bits, and

selection circuitry having a number of selection inputs equal to said number of parallel outputs of said at least one shift register, and having a number of selection outputs equal to said first number of bits, said selection inputs being connected to said parallel outputs of said at least one shift register; wherein:

said control circuitry controls which of said selection inputs is connected to said selection outputs.

41. (new) The programmable logic device of claim 40 wherein said selection circuitry is a barrel shifter.

42. (new) The programmable logic device of claim 40 wherein said second number of bits is twice said first number of bits.

43. (new) The programmable logic device of claim 42 wherein said at least one shift register comprises two shift registers chained serially, each of said shift registers having capacity to hold said first number of bits.

44. (new) A digital processing system comprising:

processing circuitry;

a memory coupled to said processing circuitry; and

a programmable logic device as defined in claim 38 coupled to the processing circuitry and the memory.

45. (new) A printed circuit board on which is mounted a programmable logic device as defined in claim 38.

46. (new) The printed circuit board defined in claim 45 further comprising:

memory circuitry mounted on the printed circuit board and coupled to the programmable logic device.

47. (new) The printed circuit board defined in claim 46 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the memory circuitry.

48. (new) A serial data interface for use with a programmable logic device having a programmable logic core, said serial data interface being adapted to receive and deserialize a serial data signal, said serial data interface comprising:

bit-slipping circuitry adapted to insert a byte boundary between bits of said deserialized serial data signal, said bit-slipping circuitry being responsive to a bit-slipping control signal from said programmable logic core.

49. (new) The serial data interface of claim 48 wherein said bit-slipping circuitry comprises bit-handling circuitry and control circuitry that controls said bit-handling circuitry responsive to said bit-slipping control signal.

50. (new) The serial data interface of claim 49 wherein:

each byte includes a first number of bits; and

said bit-handling circuitry comprises:

at least one shift register for receiving said serial data, and having capacity to hold a second number of bits greater than said first number of bits, and further having a number of parallel outputs equal to said second number of bits, and

selection circuitry having a number of selection inputs equal to said number of parallel outputs of said at least one shift register, and having a number of selection outputs equal to said first number of bits, said selection inputs being connected to said parallel outputs of said at least one shift register; wherein:

said control circuitry controls which of said selection inputs is connected to said selection outputs.

51. (new) The serial data interface of claim 50 wherein said selection circuitry is a barrel shifter.

52. (new) The serial data interface of claim 50 wherein said second number of bits is twice said first number of bits.

53. (new) The serial data interface of claim 52 wherein said at least one shift register comprises two shift registers chained serially, each of said shift registers having capacity to hold said first number of bits.

54. (new) A programmable logic device comprising the serial data interface of claim 48.

55. (new) A digital processing system comprising:

processing circuitry;

a memory coupled to said processing circuitry; and

a programmable logic device as defined in claim 54 coupled to the processing circuitry and the memory.

56. (new) A printed circuit board on which is mounted a programmable logic device as defined in claim 54.

57. (new) The printed circuit board defined in claim 56 further comprising:

memory circuitry mounted on the printed circuit board and coupled to the programmable logic device.

58. (new) The printed circuit board defined in claim 57 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the memory circuitry.